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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,033	11/27/2001	Sam Y. Guo	YAZ-157-A	9670

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EXAMINER

DEBERADINIS, ROBERT L

ART UNIT	PAPER NUMBER
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2836

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/995,033

Applicant(s)

GUO, SAM Y.

Examiner

Robert DeBeradinis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 November 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over BILOTTI 5,457,364 in view of LEE 6,194,990.

Regarding claim 1.

BILOTTI discloses a control circuit of the type comprising a power supply, a shunt resistor (60) and a controllable high speed solid state switch device (transistors 12, 18, 14, 16) for connecting the power to a load (26):

A detector (62) having inputs connected across the shunt resistor (60) and an output connected to control the state of the switch device.

BILOTTI does not disclose said shunt resistor comprising an insulated support having parallel opposite faces, and first and second electrically continuous conductor traces disposed in overlying relationship on said opposite faces.

LEE discloses a thin-film metal resistor suitable for a multilayer printed circuit board the resistor comprising an insulated support having parallel opposite faces, and first and second electrically continuous conductor traces disposed in overlying

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relationship on said opposite faces resulting in a resistor with very low self-inductance (abstract).

It would have been obvious to one having ordinary skill in the art at the time of this invention to modify the teachings of BILOTTI to include a thin-film metal shunt resistor suitable for a multiplayer printed circuit board the shunt resistor comprising an insulated support having parallel opposite faces, and first and second electrically continuous conductor traces disposed in overlying relationship on said opposite faces. The motivation would be to reduce the circuit size by having the shunt resistor (60) integrated into the multi-layered board without having the parasitic inductance associated with the discrete shunt resistor (LEE, abstract).

Regarding claim 2.

BILOTTI in view of LEE disclose the circuit as defined in claim 1.

BILOTTI teaches wherein the detector is a comparator (62).

Regarding claims 5, 6.

BILOTTI in view of LEE disclose the circuit as defined in claim 1.

LEE discloses wherein the first and second traces have multi legs on each of said faces (figure 2).

It would be obvious to have multi legs or multiple traces to form the shunt resistor. The motivation would be to configure the shunt resistor to fit on the multi layered board.

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Regarding claim 7.

BILOTTI in view of LEE teach all the limitations of claim 7 except for the milliohmic shunt resistor.

The Examiner takes official notice. It is well known that the resistance value of the shunt resistor should be small to hold its power dissipation at a minimum and large enough to produce the desired voltage to detect the desired current limit condition.

It would have been obvious to one having ordinary skill in the art at the time of this invention to select a milliohmic shunt resistor. The motivation would be to keep the power loss of the shunt resistor to a minimum.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over BILOTTI 5,457,364 in view of LEE 6,194,990 in further view of POLLERSBECK 5,914,545

Regarding claim 3.

BILOTTI in view of LEE disclose the circuit as defined in claim 1.

BILOTTI in view of LEE do not teach wherein the detector is an electronic amplifier.

POLLERSBECK teaches wherein the detector uses an electronic amplifier (15) to compare voltage levels.

It would have been obvious to one having ordinary skill in the art at the time of this invention to modify BILOTTI with the comparator taught by POLLERSBECK. The motivation would be to use an amplifier if a comparator was not available.

Regarding claim 4.

BILOTTI in view of LEE in further view of POLLERSBECK disclose the circuit as defined in claim 3.

BILOTTI teaches bridge control logic having an output connected to the switch device (bridge circuit).

BILOTTI does not teach wherein the control circuit further including a micro controller having an output connected to the switch device and an input connected to receive the output of the electronic amplifier; and the micro controller being operative to control the state of the switch device according to a signal developed across the shunt resistor.

POLLERSBECK discloses wherein the control circuit further including a micro controller (9A) having an output connected to the switch device and an input connected to receive the output of the electronic amplifier (15); and the micro controller being operative to control the state of the switch device according to a signal developed across the shunt resistor.

It would have been obvious to one having ordinary skill in the art at the time of this invention to modify the disclosure of BILOTTI to include in place of the bridge control logic a micro controller. The motivation would be to provide a controller that is software controlled for the conveyance of having control flexibility.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over POLLERSBECK 5,914,545 in view of LEE 6,194,990.
Regarding claim 8.

POLLERSBECK discloses a detector (DT) having inputs connected across the shunt resistor and an output which changes state in accordance with voltages developed across the shunt resistor; a micro-controller (9A) having an input connected to receive the output of the detector and being programmed to provide an output which changes state in accordance with a change in state of the detector output; and a FET driver (output stage of micro-controller) connected to receive the output of the micro-controller for controlling the state of the FET switch.

POLLERSBECK does not disclose wherein said shunt resistor comprises a dielectric support with first and second conductive traces printed in overlying parallel relationship on opposite faces thereof and an electrical connector extending through the support and electrically connecting the traces at one end thereof.

LEE discloses wherein said shunt resistor comprises a dielectric support with first and second conductive traces printed in overlying parallel relationship on opposite faces thereof and an electrical connector extending through the support and electrically connecting the traces at one end thereof.

It would have been obvious to one having ordinary skill in the art at the time of this invention to use the thin-film resistor disclosed by LEE for the shunt resistor. The motivation would be to develop an integrated circuit with the shunt resistor as part of the integrated board.

Regarding claims 9, 10.

POLLERSBECK in view of LEE disclose the circuit as defined in claim 8.

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LEE discloses wherein the first and second traces have multi legs on each of said faces (figure 2).

It would be obvious to have multi legs or multiple traces to form the shunt resistor. The motivation would be to configure the shunt resistor to fit on the multi layered board.

Regarding claim 11.

POLLERSBECK in view of LEE disclose the circuit as defined in claim 8.

POLLERSBECK discloses wherein the detector is an amplifier.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over POLLERSBECK 5,914,545 in view of LEE 6,194,990 in further view of BILOTTI 5,457,364.

Regarding claim 12.

POLLERSBECK in view of LEE disclose the circuit as defined in claim 8.

POLLERSBECK in view of LEE do not disclose wherein the detector is a comparator.

BILOTTI discloses wherein the detector is a comparator (62).

It would have been obvious to one having ordinary skill in the art at the time of this invention to modify POLLERSBECK with the comparator taught by BILOTTI. The motivation would be to use a comparator if an amplifier was not available.

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Any inquiry concerning this communication should be directed to Robert L. DeBeradinis whose number is (703) 306- 5857. The Examiner can normally be reached Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Brian Sircus, can be reached on (703) 308-3119. The Fax phone number for this Group is (703) 308-7722.

RLD

DECEMBER 5, 2003

A handwritten signature in cursive script, appearing to read "Robert L. DeBeradinis".